Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (original) In a memory controller, for use in a programmable logic device for connection to an external memory device, a method of performing a prefetch operation, the method comprising:

testing whether a present read access request is such that there is a high probability that said present read access request relates to configuration data for said programmable logic device; and

performing a prefetch operation only if it is determined that there is a high probability that said present read access request relates to configuration data for said programmable logic device.

2. (original) A method as claimed in claim 1, wherein the step of testing whether a present read access request is such that there is a high probability that said present read access request relates to configuration data for said programmable logic device comprises:

determining whether the present read access request relates to a burst type from a predetermined group of suitable burst types, selected from the possible burst types.

3. (original) A method as claimed in claim 2, wherein the predetermined group of suitable burst types comprises defined length accesses.

4. (original) A method as claimed in claim 1, further comprising, if it is determined that a prefetch operation is to be performed:

when the present read access request is completed, testing whether a read buffer contains an amount of unused space exceeding a predetermined threshold; and

performing the prefetch operation only if it determined that the read buffer contains an amount of unused space exceeding a predetermined threshold.

5. (original) A method as claimed in claim 4, further comprising prefetching a predetermined amount of data.

6. (original) A method as claimed in claim 5, wherein said predetermined threshold for said amount of unused space in the read buffer corresponds to said predetermined amount of data.

7. (original) A method as claimed in claim 5, further comprising, after prefetching said predetermined amount of data:

testing whether said read buffer still contains an amount of unused space exceeding said predetermined threshold; and

continuing a prefetch operation only if it determined that the read buffer still contains an amount of unused space exceeding said predetermined threshold.

8. (original) A method as claimed in claim 7, further comprising prefetching a further predetermined amount of data.

9. (original) A method as claimed in claim 2, further comprising, if a further read access request is received while a prefetch operation is in progress:

determining whether said further read access request relates to a burst type from said predetermined group of suitable burst types; and

terminating said prefetch operation if said further read access request does not relate to a burst type from said predetermined group of suitable burst types.

10. (original) A method as claimed in claim 9, further comprising, if a further read access request is received while a prefetch operation is in progress, and if said further read access request does not relate to a burst type from said predetermined group of suitable burst types:

flushing prefetched data from a read buffer, and subsequently performing the operation requested in said further read access request.

11. (original) A method as claimed in claim 9, further comprising continuing said prefetch operation, and returning prefetched data to a requesting device, only if a start address of said further read access request corresponds to a start address of said prefetch operation which is in progress.

12. (original) A programmable logic device, comprising:

a configuration memory, for storing configuration data; and

a memory controller, for connection to an external memory device, wherein, when said memory controller receives a present read access request, said memory controller retrieves the data requested in said present read access request, and determines whether said present read access request is such that there is a high probability that said present read access request relates to configuration data for said programmable logic device; and

said memory controller performs a prefetch operation after completing retrieval of the data requested in said present read access request only if it is determined that there is a high probability that said present read access request relates to configuration data for said programmable logic device.

13. (original) An electronic system, comprising a programmable logic device and an external memory device, wherein said programmable logic device comprises:

a configuration memory, for storing configuration data; and

a memory controller, for connection to said external memory device, wherein, when said memory controller receives a present read access request, said memory controller retrieves the data requested in said present read access request, and determines whether said present read access request is such that there is a high probability that said present read access request relates to configuration data for said programmable logic device; and

said memory controller performs a prefetch operation after completing retrieval of the data requested in said present read access request only if it is determined that there is a high

probability that said present read access request relates to configuration data for said programmable logic device.

14. (original) An electronic system as claimed in claim 13, wherein said external memory device comprises a flash memory device.

15. (original) An electronic system as claimed in claim 13, wherein said external memory device comprises a SRAM device.

16. (canceled)

17. (new) A programmable logic device as claimed in claim 12, wherein said memory controller determines whether said present read access request is in the form of a defined length burst.

18. (new) A programmable logic device as claimed in claim 12, wherein said memory controller performs a prefetch operation after completing retrieval of the data requested in said present read access request only if it is determined that a read buffer contains an amount of unused space exceeding a predetermined threshold.

19. (new) A programmable logic device as claimed in claim 12 wherein, if a further read access request is received while a prefetch operation is in progress, said memory controller returns prefetched data to a requesting device if:

the further read access request relates to a defined length burst;

the further read access request corresponds to a same chip select of said prefetch operation which is in progress; and

the start address of said further read access request corresponds to a start address of said prefetch operation which is in progress.

20. (new) An electronic system as claimed in claim 13, wherein said memory controller determines whether said present read access request is in the form of a defined length burst.

21. (new) An electronic system as claimed in claim 13, wherein said memory controller performs a prefetch operation after completing retrieval of the data requested in said present read access request only if it is determined that that buffer space is available.

22. (new) An electronic system as claimed in claim 13, wherein, if a further read access request is received while a prefetch operation is in progress, said memory controller returns prefetched data to a requesting device if:

the further read access request relates to a defined length burst;

the further read access request corresponds to a same chip select of said prefetch operation which is in progress; and

the start address of said further read access request corresponds to a start address of said prefetch operation which is in progress.